WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a memory;

an ECC circuit that has an error correction function of N (N is a natural number) bits for output data of the memory; and

an error detection circuit configured to output a signal indicative of the following fact, if a total of an error bit number n1 detected by the ECC circuit when a first data pattern in testing target addresses of the memory is read out and an error bit number n2 detected by the ECC circuit when a second data pattern that is an inversion of the first data pattern in at least a part of the testing target addresses is read out exceeds N.

2. The semiconductor integrated circuit according to claim 1, further comprising:

a BIST circuit configured to read the first data pattern out of the testing target addresses of the memory as a first operation, write the second pattern in at least a part of the testing target addresses as a second operation, and read out the written second data pattern.

3. The semiconductor integrated circuit according to claim 2,

wherein the BIST circuit repeats the first and second operations while changing the testing target

addresses.

4. The semiconductor integrated circuit according to claim 3,

wherein the BIST circuit writes the first data pattern as background data in all the addresses of the memory before the first and second operations are repeated.

5. The semiconductor integrated circuit according to claim 2, wherein:

the ECC circuit outputs SEC signals indicative of the error bit numbers n1 and n2;

the BIST circuit outputs a first reading signal during reading of the first data pattern, and a second reading signal during reading of the second data pattern; and

the error detection circuit stores the error bit number n1 upon reception of the first reading signal, and the error bit number n2 upon reception of the second reading signal, and calculates n1+n2 by logic processing.

6. The semiconductor integrated circuit according to claim 5,

wherein the error bit numbers n1 and n2 are stored in registers.

7. The semiconductor integrated circuit according to claim 1,

wherein the error detection circuit sets only

a bit among bits of the testing target addresses in which the second data pattern has been written to be checked, and counts in the error bit number n2 for an error generated in the bit to be checked.

8. The semiconductor integrated circuit according to claim 7,

wherein the testing target addresses contain data bits and code bits, and bits other than the bit to be checked are parts of the data bits.

9. The semiconductor integrated circuit according to claim 7,

wherein the testing target addresses contain data bits and code bits, and bits other than the bit to be checked are parts of the code bits.

10. The semiconductor integrated circuit according to claim 7, wherein:

the ECC circuit outputs an SEC signal indicative of presence of an error to each of the bits of the testing target addresses;

the BIST circuit outputs a state signal indicative of the first and second test patterns; and

the error detection circuit specifies the bit to be checked based on the state signal, and obtains the error bit number n2 for the bit to be checked based on the SEC signal.

11. The semiconductor integrated circuit according to claim 1,

wherein the N is 1.

12. The semiconductor chip according to claim 10,

wherein the semiconductor integrated circuit constitutes a part of a system LSI.

13. A test method of a semiconductor memory with an ECC circuit comprising:

reading a first data pattern out of testing target addresses of a memory;

detecting an error bit number n1 by using the ECC circuit that has an error correction function of N (N is a natural number) bits;

writing/reading a second data pattern that is an inversion of the first data pattern in at least a part of the testing target addresses;

detecting an error bit number n2 by using the ECC circuit; and

determining whether a total of the error bit numbers n1 and n2 exceeds N or not.

14. The test method according to claim 13,

wherein after the first data pattern is written as background data in all the addresses of the memory, the reading of the first data pattern and the writing/reading of the second data pattern are repeated while the testing target addresses are changed.

15. The test method according to claim 13,

wherein the error bit numbers n1 and n2 are stored in registers.

16. The test method according to claim 13,

wherein only a bit among the bits of the testing target addresses in which the second data pattern has been written is set to be checked, and the error bit number n2 is counted in for an error generated in the bit to be checked.

17. The test method according to claim 16,

wherein the ECC circuit determines presence of an error for each of the bits of the testing target addresses.

18. The test method according to claim 16,

wherein the bit to be checked is specified based on the first and second data patterns.

19. The test method according to claim 13,

wherein the first and second data patterns are generated in a chip.

20. The test method according to claim 12,

wherein the semiconductor integrated circuit is determined to be a defective product when a total of the error bit numbers n1 and n2 exceeds N.